IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 3, between lines 24-25 of the specification with the following:

Figure 7 is a block diagram illustrating an alternative embodiment of an adaptive signal ~~processing~~ processor;

Replace the paragraph on page 8, between lines 15-19 of the specification (also amended by the Amendment of September 25, 2008) with the following:

The second delay calculator 130 has a first input 131 coupled to the output 112C of the third controllable filter device ~~110B~~ 110C, and has a second input 132 coupled to the output 112B of the fourth controllable filter device 110B. At its output 133, the second delay calculator 130 provides a signal S2 representing the delay $\Delta(B,C)$ between the signals B and C of the second and third detector segments 35b and 35c, respectively.

Replace the paragraph on page 13, between lines 14-18 of the specification with the following:

In figures 4 and 7, this functionality is illustrated as a signal S, which is fed to sign inputs 124, 134, 324, 334, 424, 434 of the delay calculators 120, 130, 320, 330, 420, 430, respectively. This signal S may be equal to, or derived from, the output filter control signal S_{FC} from the filter controller 160. In an embodiment, ~~s equals~~ S equals +1 in the presence of data, and ~~s equals~~ S equals -1 in the absence of data.